Features

- **High-performance DirectSound™ Direct3DSound™ Operation**
  - **Direct Access to Audio Data as PCI Master**
  - **Uses PCI Bursts with Patented Proprietary Cache RAM to Minimize PCI Bandwidth**
  - **Mixes up to 64 Audio Channels at 48 kHz (Streaming Audio and/or Static Buffers)**
  - **Up to Eight Audio Channels in Record**
  - **Interactive Audio Includes per Channel Doppler, 4-speaker Output and Filter**
  - **Audio Effects: Reverb, Chorus, Echo, Pitch Shifting, 4-band Equalizer, Surround**
- **Top-quality Wavetable Synthesis**
  - **16-bit Samples @ 48 kHz Sampling Rate**
  - **Up to 64-voice Polyphony by Hardware**
  - **Internal Computations on 28 Bits, DAC Support up to 22 Bits**
  - **Alternate Loop, 24 dB Digital Filter for Each Voice**
  - **Roland GS™ Format-compliant**
  - **Sample Sets under Roland® License, rSounds © Roland Corporation 1996**
  - **DirectMusic™ Accelerator, Downloadable Sounds DLS1 Support, DLS2 Ready**
- **Multiple Audio Inputs and Outputs**
  - **AC97 Codec-compliant Interface**
  - **Three I2S Outputs (Six Audio Channels)**
  - **Four I2S inputs (Eight Audio Channels)**
  - **Home PC-ready for Dolby® AC-3 Six-speaker output**
  - **Dual Joystick Game Port**
- **Multi-platform**
  - **Windows® 95/98 Drivers**
  - **Windows® 2000 WDM Drivers**
- **Fully Programmable**
  - **Firmware Resides in PC Memory and in On-chip RAM**
  - **Evolutive Firmware Open to Third-party Developers**
- **Designed for PC Motherboards and Notebooks**
  - **3.3V or 5V Operation**
  - **Choice of Standard 100-lead PQFP or Space-saving 100-lead TQFP Package**

Description

The highly-integrated architecture of SAM9777 is derived from the SAM9407 but contains significant improvements.

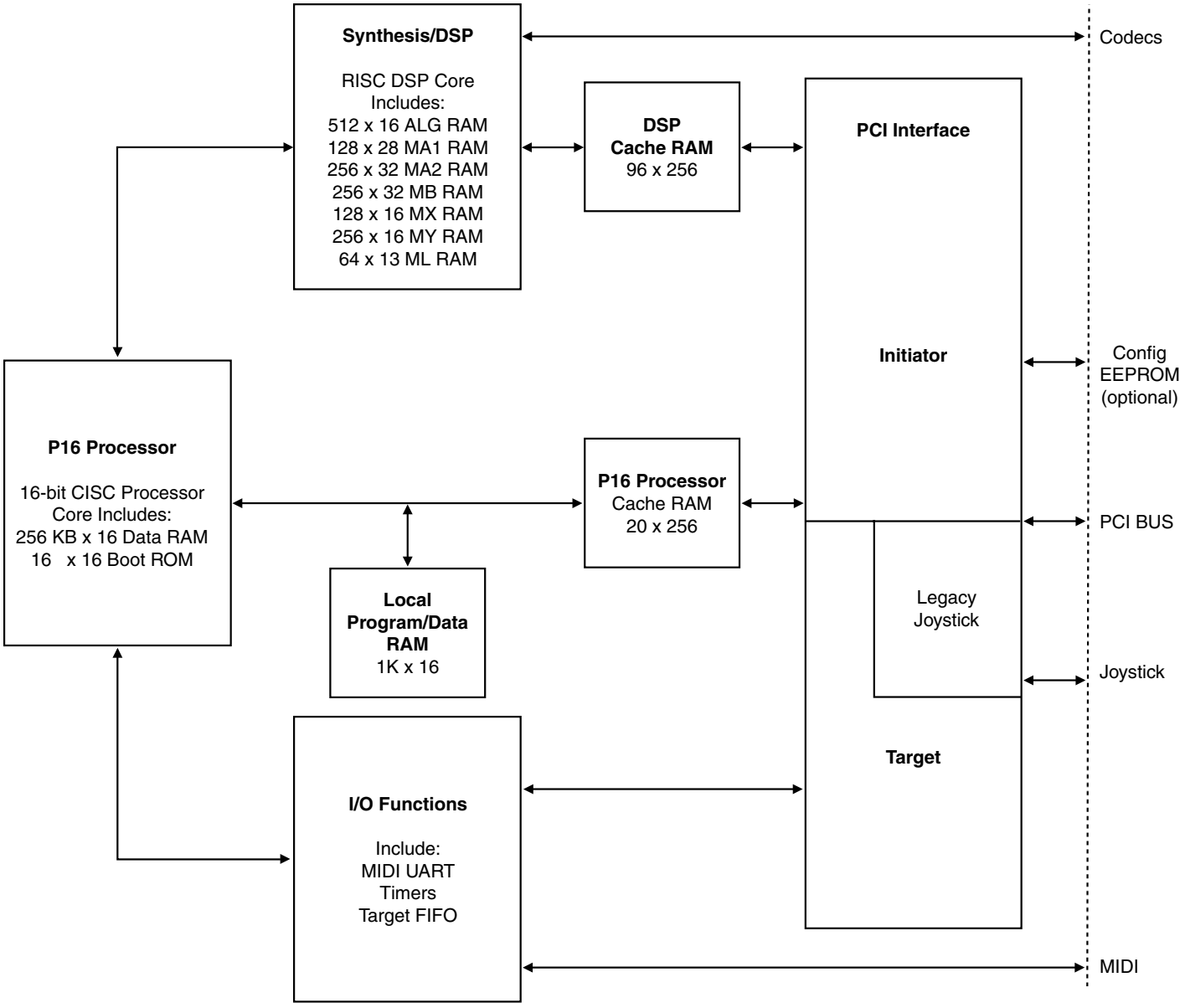
The SAM9777 combines a specialized high-performance RISC-based digital signal processor (synthesis/DSP) and a general-purpose 16-bit CISC-based control processor on a single chip. A PCI interface with bus mastering capability allows the synthesis/DSP and the control processor to directly access external PC memory. A local program/data RAM, independent synthesis/DSP and control processor cache RAM, as well as PCI transfers on a PC CPU-cache line basis allow a dramatic reduction in PCI bandwidth. An intelligent peripheral I/O interface function handles other I/O interfaces such as controls received from the PCI interface in target mode, the on-chip MIDI UART, and three timers with minimum intervention from the control processor. The PCI interface also implements a legacy joystick.

PCI Bus Single-chip Multimedia Sound System

SAM9777

Rev. 1716A–03/01

Figure 1. Functional Overview Block Diagram



Pin Description

PCI Bus Group

Table 1. PCI Bus Group (All signals PCI-compliant)

Pin Name	Pin Count	Type	Function
AD[31:0]	32	I/O	Multiplexed address/data
$\overline{\text{C/BE[3:0]}}$	4	I/O	Command and byte enables
PAR	1	I/O	Parity
$\overline{\text{FRAME}}$	1	I/O	Cycle Frame
$\overline{\text{IRDY}}$	1	I/O	Initiator ready
$\overline{\text{TRDY}}$	1	I/O	Target ready
$\overline{\text{STOP}}$	1	IN	Indicates target requests SAM9777 to stop transaction
$\overline{\text{DEVSEL}}$	1	I/O	Device select
IDSEL	1	IN	Initialization device select
$\overline{\text{PERR}}$	1	I/O	Parity error
$\overline{\text{REQ}}$	1	TS OUT	Request bus for master operation
$\overline{\text{GNT}}$	1	IN	Master access to bus granted
CLK	1	IN	PCI timing clock
$\overline{\text{RST}}$	1	IN	System reset
$\overline{\text{INTA}}$	1	OD	Open drain signal, interrupt request

Digital Audio Group

Table 2. Digital Audio Group

Pin Name	Pin Count	Type	Function
$\overline{\text{AC\_RES}}$	1	OUT	AC 97 Master reset, can also be used as buffered $\overline{\text{RESET}}$ for DAC/ADC
AC_SYNC	1	OUT	AC 97 48 kHz fixed sampling rate
AC_DOUT SD_OUT_0	1	OUT	Multi-function pin. Configured by firmware. Serial audio stream to AC 97 or I2S data out channel 0.
AC_DIN SD_IN_0	1	IN	Multi-function pin. Configured by firmware. Serial audio stream from AC 97 or I2S data in channel 0.
BCK_OUT	1	OUT	I2S bit clock for audio-out and master mode audio-in
WS_OUT	1	OUT	Multi-function pin. Output, I2S data word select for audio-out and audio-in.
SD_OUT_1	1	OUT	Multi-function pin. Output I2S auxiliary stereo-out channel #1 data @ 32 bits per sample (22 useful bits).
SD_OUT_2	1	OUT	Multi-function pin. Output I2S auxiliary stereo-out channel #2 data @ 32 bits per sample (22 useful bits).

Table 2. Digital Audio Group (Continued)

Pin Name	Pin Count	Type	Function
SD_IN_1P1	1	IN or I/O	Multi-function pin. Configuration by firmware. I2S data in channel 1 or general-purpose I/O pin.
SD_IN_2P2	1	IN or I/O	Multi-function pin. Configuration by firmware. I2S data in channel 2 or general-purpose I/O pin.
SD_IN_3P3	1	IN or I/O	Multi-function pin. Configuration by firmware. I2S data in channel 3 or general-purpose I/O pin.

Joystick, MIDI and Miscellaneous Group

Table 3. Joystick, MIDI and Miscellaneous Group

Pin Name	Pin Count	Type	Function
JSX1, JSY1	2	AIN	Joystick 1 coordinates
JSB11, JSB12	2	IN	Joystick 1 buttons 1 & 2
JSX2, JSY2	2	AIN	Joystick 2 coordinates
JSB21, JSB22	2	IN	Joystick 2 buttons 1 & 2
JSREF	1	AIN	Joystick reference voltage
MIDI IN	1	IN	Serial MIDI-IN
MIDI OUT	1	OUT	Serial MIDI-OUT
P0	1	I/O or OD	Multi-function pin. General-purpose I/O pin
CKIN	1	–	12.288 MHz master clock input (256xFs). Normally connected to AC 97 BIT_CLK
LFT	1	–	PLL decoupling
TEST0, TEST1	1	IN	Test pins, should be grounded for normal operation.
SCL, SDA	1		Optional Serial configuration EEPROM connection.

Power Supply Group

Table 4. Power Supply Group

Pin Name	Pin Count	Function
GND	9	Digital ground pins. All pins should be connected to a ground plane below the IC.
VC3	9	3.3V ± 10% digital power. All pins should be connected.
VCC	1	3V to 5.5V periphery power. Determines the operation level of the Codec EEPROM and MIDI signals.
AGND	1	Analog ground for the joystick analog pins JSXn/JSYn
AVC3	1	Analog power for the joystick pins JSXn/JSYn, 3.3V ± 10%

Pinout by Pin

Table 5. Pinout for 100-lead PQFP Package (ref. SAM9777-PQ)

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
1	AD20	26	AD10	51	VCC	76	$\overline{\text{RST}}$
2	GND	27	AD9	52	GND	77	CLK
3	GND	28	VC3	53	GND	78	VC3
4	AD18	29	VC3	54	SD_OUT_2	79	VC3
5	AD17	30	AD8	55	SD_OUT_1	80	$\overline{\text{GNT}}$
6	AD16	31	$\overline{\text{C/BE0}}$	56	WS_OUT	81	$\overline{\text{REQ}}$
7	$\overline{\text{C/BE2}}$	32	GND	57	BCK_OUT	82	NC
8	$\overline{\text{FRAME}}$	33	AD7	58	$\overline{\text{AC\_RES}}$	83	GND
9	$\overline{\text{IRDY}}$	34	AD6	59	AC_SYNC	84	GND
10	$\overline{\text{TRDY}}$	35	AD5	60	AC_DIN, SD_IN_0	85	AD31
11	GND	36	AD4	61	CKIN	86	AD30
12	VC3	37	AD3	62	AC_DOUT, SD_OUT_0	87	AD29
13	VC3	38	VC3	63	JSB22	88	AD28
14	$\overline{\text{DEVSEL}}$	39	AD2	64	JSB21	89	AD27
15	$\overline{\text{STOP}}$	40	AD1	65	JSB12	90	VC3
16	TEST1	41	AD0	66	JSB11	91	AD26
17	$\overline{\text{PERR}}$	42	SCL	67	AGND	92	AS25
18	PAR	43	SDA	68	JSY2	93	AD24
19	$\overline{\text{C/BE1}}$	44	TEST0	69	JSX2	94	$\overline{\text{C/BE3}}$
20	AD15	45	P0	70	JSREF	95	IDSEL
21	AD14	46	SD_IN_1, P1	71	JSY1	96	AD23
22	GND	47	SD_IN_2, P2	72	JSX1	97	AD22
23	AD13	48	SD_IN_3, P3	73	AVC3	98	VC3
24	AD12	49	MIDI OUT	74	$\overline{\text{INTA}}$	99	AD21
25	AD11	50	MIDI IN	75	LFT	100	AD20

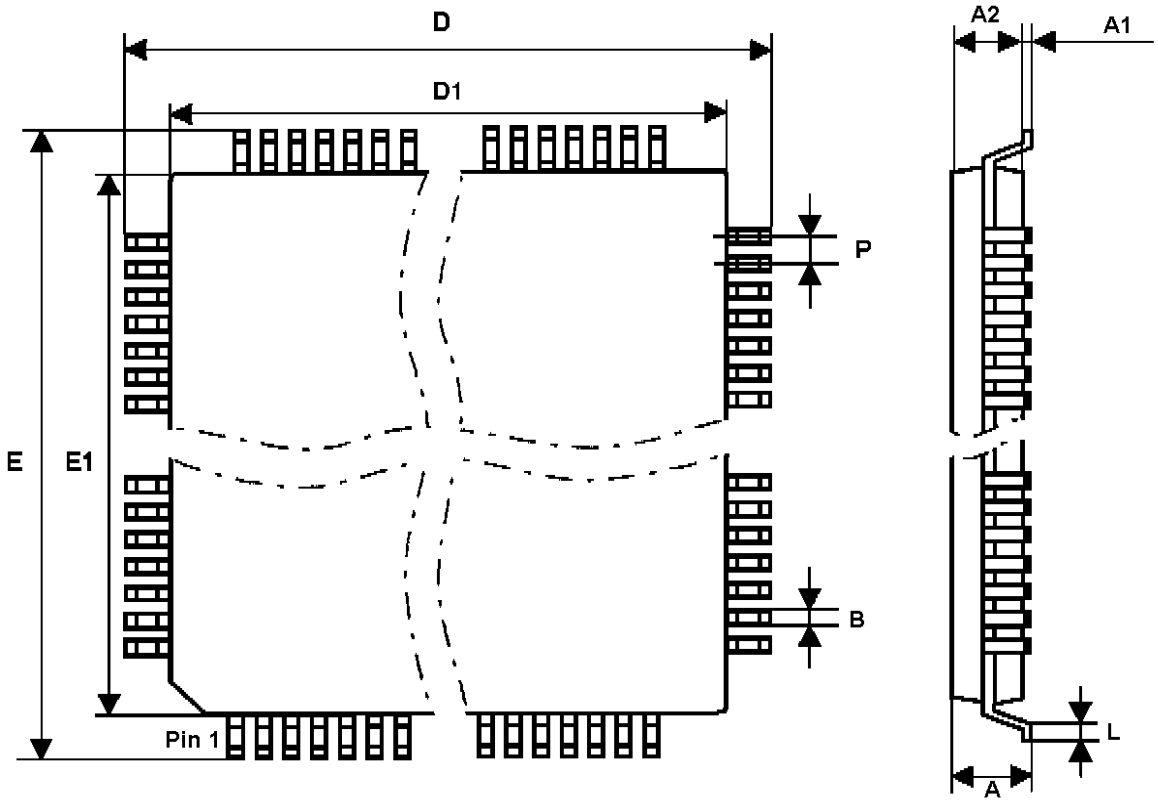
.

Table 6. Pinout for Space-saving 100-lead TQFP Package (ref SAM9777-TQ)

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
1	GND	26	VC3	51	GND	76	VC3
2	AD18	27	VC3	52	SD_OUT_2	77	VC3
3	AD17	28	AD8	53	SD_OUT_1	78	$\overline{\text{GNT}}$
4	AD16	29	$\overline{\text{C/BE0}}$	54	WS_OUT	79	$\overline{\text{REQ}}$
5	$\overline{\text{C/BE02}}$	30	GND	55	BCK_OUT	80	$\overline{\text{PME}}$
6	$\overline{\text{FRAME}}$	31	AD7	56	$\overline{\text{AC\_RES}}$	81	GND
7	$\overline{\text{IRDY}}$	32	AD6	57	AC_SYNC	82	GND
8	$\overline{\text{TRDY}}$	33	AD5	58	AC_DIN, SD_IN_0	83	AD31
9	GND	34	AD4	59	CKIN	84	AD30
10	VC3	35	AD3	60	AC_DOUT, SD_OUT_0	85	AD29
11	VC3	36	VC3	61	JSB22	86	AD28
12	$\overline{\text{DEVSEL}}$	37	AD2	62	JSB21	87	AD27
13	$\overline{\text{STOP}}$	38	AD1	63	JSB12	88	VC3
14	TEST1	39	AD0	64	JSB11	89	AD26
15	$\overline{\text{PERR}}$	40	SCL	65	AGND	90	AS25
16	PAR	41	SDA	66	JSY2	91	AD24
17	$\overline{\text{C/BE1}}$	42	TEST0	67	JSX2	92	$\overline{\text{C/BE3}}$
18	AD15	43	P0	68	JSREF	93	IDSEL
19	AD14	44	SD_IN_1, P1	69	JSY1	94	AD23
20	GND	45	SD_IN_2, P2	70	JSX1	95	AD22
21	AD13	46	SD_IN_3, P3	71	AVC3	96	VC3
22	AD12	47	MIDI OUT	72	$\overline{\text{INTA}}$	97	AD21
23	AD11	48	MIDI IN	73	LFT	98	AD20
24	AD10	49	VCC	74	$\overline{\text{RST}}$	99	AD19
25	AD9	50	GND	75	CLK	100	GND

Mechanical Dimensions

Figure 2. 100-lead Plastic Quad Flat Pack – Rectangular



Package Dimensions (in millimeters)

Table 7. 100-lead Plastic Quad Flat Pack – Rectangular

Dimension	Min	Typ	Max
A			3.40
A1	0.25		
A2	2.55	2.8	3.05
D		23.90	
D1		20.00	
E		17.90	
E1		14.00	
L	0.65	0.88	1.03
P		0.65	
B	0.22		0.38

Table 8. 100-lead Thin PQFP Package – Square

Dimension	Min	Typ	Max
A	1.40	1.50	1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
D		16.00	
D1		14.00	
E		16.00	
E1		14.00	
L	0.45	0.60	0.75
P		0.65	
B	0.17	0.22	0.27

Absolute Maximum Ratings

Table 9. Absolute Maximum Ratings

Symbol	Parameter/Condition	Min	Typ	Max	Unit
	Ambient Temperature (Power applied)	-40		+85	°C
	Storage Temperature	-6.5		+150	°C
	Voltage on any pin	-0.5		V_{CC} + 0.5	V
V_{CC}	Supply Voltage	-0.5		6.5	V
AV_{C3}, V_{C3}	Supply Voltage	-0.5		4.5	V
	Maximum I_{OL} per I/O pin			10	mA

Note: All voltages with respect to 0V, GND = 0V.

Recommended Operating Conditions

Table 10. Recommended Operating Conditions

Symbol	Parameter/Condition	Min	Typ	Max	Unit
V_{CC}	Supply Voltage[1]	3	3.3/5.0	5.5	V
V_{C3}	Supply Voltage	3	3.3	3.7	V
T_A	Operating Ambient Temperature	0		70	°C

Note: 1. When using 3.3V supply, care must be taken that voltage applied on pin does not exceed V_{CC} + 0.5V.

DC Characteristics

Table 11. DC Characteristics (T_A = 25°C, V_{C3} = 3.3V ± 10%)

Symbol	Parameter/Condition	V_{CC}	Min	Typ	Max	Unit
V_{IL}	Low-level Input Voltage	3.3 5.0	-0.5 -0.5		1.0 1.7	V V
V_{IH}	High-level Input Voltage	3.3 5.0	2.3 3.3		3.8 5.5	V V
I_{CC}	Power Supply Current	3.3 5.0		TBD		mA mA
	Power Down Supply Current			TBD		µA

Functional Overview

Synthesis/DSP Engine

The synthesis/DSP engine operates on a frame-timing basis with the frame subdivided into 64 process slots. Each process is itself divided into 16 micro-instructions known as “algorithms”. Up to 32 synthesis/DSP algorithms can be stored on-chip in the Alg RAM memory, allowing the device to be programmed for a number of audio signal generation/processing applications. The synthesis/DSP engine is capable of generating 64 simultaneous voices using algorithms such as wavetable synthesis with interpolation, alternate loop and 24 dB resonant filtering for each voice. Slots may be linked together (ML RAM) to allow implementation of more complex synthesis algorithms.

A typical multimedia application will use part of the capacity of the synthesis/DSP engine for fixed resource functions such as reverberation, chorus, echo, pitch-shifting, surround, equalizer, etc. The remaining capacity will typically be dynamically allocated between direct-sound play/record and wavetable synthesis. With all fixed-resource functions removed, 64-voice synthesis or 32 direct-sound channels can be achieved.

Frequently-accessed synthesis/DSP parameter data are stored in five banks of on-chip RAM memory. Sample data or delay lines that are accessed relatively infrequently are stored in external PC memory and accessed through the synthesis/DSP cache RAM. The combination of localized micro-program memory and localized parameter data allows micro-instructions to execute in 20 ns (50 MIPS).

Separate buses from each of the on-chip parameter RAM memory banks allow highly-parallel data movement to increase the effectiveness of each micro-instruction. With this architecture, a single micro-instruction can accomplish up to eight simultaneous operations (add, multiply, load, store, etc.), providing a potential throughput of 400 million operations per second (MOPS).

Compared to the SAM9407, the synthesis/DSP engine now offers the following significant enhancements:

- 24 x 16 multiplier
- Direct support of 8-/16-bit mono/stereo Microsoft wave formats
- No “bank” limitation
- 32-bit word size for delay lines, giving virtually noise-free reverb
- Pan steps of 0.75 dB
- Audio data in on 20 bits
- Six channels audio-out

P16 Control Processor and I/O Functions

The P16 control processor is a general-purpose 16-bit CISC processor core that runs from a local program/data RAM or from PC memory through the P16 processor cache RAM. A boot ROM is included that allows the PC to upload an initial program into the local program/data RAM at power-up. The P16 also includes 256 words of local RAM data memory. The first 16 words of this RAM hold general-purpose registers; the next eight words hold segment and I/O registers. The remaining part of the RAM is free to store frequently-used variables and the stack.

The P16 control processor writes to the parameter RAM blocks within the synthesis/DSP core in order to control the synthesis process. In a typical application, the P16 control processor parses and interprets incoming commands from the MIDI UART or from the PCI interface and then controls the synthesis/DSP by writing into the parameter RAM banks in the DSP core. Slowly-changing synthesis functions such as LFOs are implemented in the P16 control processor by periodically updating the DSP parameter RAM variables.

The P16 control processor interfaces with other peripheral devices, such as the system control and status registers, the on-chip MIDI UART, the on-chip timers and the PCI interface through specialized “intelligent” peripheral I/O logic. This I/O logic automates many of the system I/O transfers to minimize the amount of overhead processing required from the P16.

PCI Interface

The PCI interface can operate in both initiator and target mode.

In initiator mode, the PCI interface is a PCI bus master. It can access any address in the 32-bit PC RAM space. Two base registers provide different segments for the P16 program/data and the synthesis/DSP RAM. This allows simple relocation of the synthesis/DSP address space without interrupting the P16 program. Most PCI transfers occur on a PC cache line basis, i.e., as a burst of eight 32-bit words. Such a burst will typically take 13 cycles on the PCI bus, which is about 390 ns. When playing audio at 48 kHz mono 16 bits, this means that 16 audio samples are read in 390 ns, taking only 0.12% of the PCI bandwidth.

In target mode, the PCI interface is assigned I/O or memory range as defined by the plug-and-play BIOS or operating system. 16 consecutive bytes of I/O or memory space are required and a single interrupt line $\overline{\text{INTA}}$. At power-up, the legacy devices are hidden (they do not participate in the plug-and-play enumeration). A specific

configuration program is required to enable the legacy devices. Legacy devices are implemented in the PCI configuration registers according to Intel® recommendations.

An optional serial EEPROM can be connected to the SAM9777. It allows the default configuration registers setting to be overridden. This allows the SAM9777 to be customized for different vendors, giving the possibility of distinguishing a SAM9777 mounted on the motherboard from a SAM9777 mounted on an audio add-in card.

Additional Information

PCI Bus Bandwidth

The PCI bus bandwidth utilized by a PCI sound card is a major concern, as it determines critical parameters such as the number of streaming audio that can be mixed together or the maximum video frame rate for a game. Unlike most PCI sound accelerators, the SAM9777 processes everything on-chip. This includes MIDI data parsing and processing and effects like reverb, chorus, echo, equalizer, surround, filter, pitch shifting and 3-D positioning. Another unique feature of the SAM9777 device is that the built-in 16-bit processor (P16) executes instructions from a built-in local RAM and from PC memory (through a built-in cache). Thorough testing has been conducted in order to determine the PCI bus bandwidth utilization of such a structure.

The results are given in Table 12 for a worst-traffic case from a typical application.

Table 12. PCI Bus Bandwidth Instruction Execution

Functional Block	Average PCI Burst Access/Synthesis Frame
32 mono 16-bit waves @ 48 kHz, 3-D positioning	2 (read)
Reverb with 13 delay lines	0.8 (read) 0.8 (write)
Equalizer 4 bands	0
P16 (worst case = 10% out of PC memory)	0.2 (read) 0.1 (write)
Total	3 (read) 0.9 (write)

With:

- Synthesis frame = 20833 ns
- PCI burst read = 390 ns
- PCI burst write = 630 ns

This gives a total PCI load due to the SAM9777 of 8.3%. On this load, only 0.7% is related to the P16.

Note that this computation only takes into account the load due to the SAM9777 itself. The total load for audio depends on PC implementation (secondary cache size, DRAM configuration and speed) and on the software application implementation (wave data located in main memory or on disk). Also the load assumes that there are no retries on the PCI bus.

PCI Configuration Space

The reader is assumed to be familiar with the PCI bus specification as defined in the document published by the PCI Special Interest Group *PCI Local Bus Specification. Rev 2.1 June 1st, 1995.*

Configuration Space Overview

Table 13. Configuration Space Overview

00H	Device ID = 9777/EEP(1)		Vendor ID = Atmel-Dream® ID/EEP(1)	
04H	Status Register		Command Register	
08H	Class Code = 04 01 00 (Multimedia Audio)			Revision ID = 0
0CH	BIST = 00	Header Type = 00	Latency Timer	Cache Line = 00
10H	Base Memory Mode			
14H	Base I/O Mode			
18H	00 00 00 00			
1CH	00 00 00 00			
20H	00 00 00 00			
24H	00 00 00 00			
28H	00 00 00 00			
2CH	Subsystem ID = 00 00/EEP(1)		Subsystem Vendor ID = 00 00/EEP(1)	
30H	00 00 00 00			
34H	00 00 00 00			Cap_ptr = 00/EEP(1)
38H	00 00 00 00			
3CH	Max_Lat = 00	Min_Gnt = 00	Interrupt Pin = 01	Interrupt Line
40H	–		LACR	
44H	–		DMACFG	
48H	–			
4CH	–			
50H	–			
54H	–			
58H	–			
5CH	–			
60H	–			
64H	Joystick Base (default 200 - 207H)			
68H	–			
6CH	–			
70H	–			
74H	–			
78H	–			
7CH	–			

Table 13. Configuration Space Overview (Continued)

80H	–
84H	–
≥ 88H	00 00 00 00

Notes: 1. EEP means that value can be replaced by EEPROM content.
2. Addresses 00H to 3FH hold the standard PCI configuration.

Configuration Registers Description

PCI Standard Registers

Vendor ID (00H - 01H, read-only)

15	14	13	12	11	10	9	8a	7	6	5	4	3	2	1	0
1438H or EEPROM															

Identifies the manufacturer of the device. If no EEPROM is connected, then it holds the Atmel-Dream® PCI ID = 1438H, otherwise it holds bytes 2 and 3 of the EEPROM.

Device ID (02H - 03H, read-only)

15	14	13	12	11	10	9	8a	7	6	5	4	3	2	1	0
9777H or EEPROM															

Identifies the device. It reads as 9777H if no EEPROM or bytes 4 and 5 from the EEPROM.

Command (04H - 05H, partial read/write)

15	14	13	12	11	10	9	8a	7	6	5	4	3	2	1	0
Reserved						0	0	0	0	0	0	0	BM	MS	IO

Bits IO, MS, BM are read/write, all other bits are read-only and return zero.

- IO: If 1, allows the device to respond to I/O space accesses (reads zero after reset).
- MS: If 1, allows the device to respond to memory space accesses (reads zero after reset).
- BM: If 1, allows the device to act as a master on the PCI bus (reads zero after reset).

Status (06H - 07H, partial read/write)

15	14	13	12	11	10	9	8a	7	6	5	4	3	2	1	0
DPE	SSE	RMA	RTA	STA	Speed		MPE	BTB	UDF	66M	Reserved				

- Reserved: read-only, returns 00000
- 66M: 66 MHz-capable, read-only, returns zero
- UDF: UDF supported, read-only, returns zero
- BTB: Fast back-to-back capable, read-only, returns zero
- MPE: Master Parity Error detected, implemented
- Speed: DEVSEL timing, read-only, returns 01 (medium speed device)

- STA: Signaled target abort, read-only, returns 0
- RTA: Received target abort, implemented
- RMA: Received master abort, implemented
- SSE: Signaled system error, read-only, returns 0
- DPE: Detected Parity Error, implemented

Note: According to the PCI specification, implemented bits can only be set by device. They can be reset by writing the corresponding bit at 1.

Revision ID (08H, read-only)

Indicates revision of device, returns 0

Class Code (09H - 0BH, read-only)

Indicates Multimedia Audio Device, returns 04H 01H, 00H

Cache Line Size (0CH, read-only)

Not applicable, returns zero

Latency Timer (0DH, read/write)

Reads zero after reset

Header Type (0EH, read-only)

Returns zero (single function device)

BIST (0FH, read-only)

BIST not supported, returns zero

Base memory mode (10H - 13H, partial read/write)

31	30	29	28	27	...	8a	7	6	5	4	3	2	1	0
Base Address											0	0	0	0

Bits 0 - 3 always read back as zero, indicating memory mode, locate anywhere in 32-bit address space, not prefetchable, size 16 bytes.

Base I/O mode (14H - 17H, partial read/write)

31	30	29	28	27	...	8a	7	6	5	4	3	2	1	0
Base Address											0	0	0	1

Bits 0 - 3 always read back as 0001, indicating I/O mode, size 16 bytes.

Subsystem Vendor ID (2CH - 2DH, read-only)

Returns zero if no EEPROM, or bytes 6 and 7 from the EEPROM

Subsystem ID (2EH - 2FH, read-only)

Returns zero if no EEPROM, or bytes 8 and 9 from the EEPROM

Interrupt Line (3CH, read/write)

Used by the operating system to indicate interrupt routing.

Interrupt Pin (3DH, read-only)

Returns 01H indicating that the device needs one interrupt ($\overline{INTA}$).

Min_Gnt (3EH, read-only)

Minimum Grant, returns zero (no major requirement).

Max_Lat (3FH, read-only)

Maximum Latency, returns zero (no major requirement).

Legacy Audio Control Registers

LACR, Legacy Audio Configuration Register (40H - 41H, read/write)

15	14	13	12	11	10	9	8a	7	6	5	4	3	2	1	0
LAD													JE		

The reset value of LACR is 907FH.

LAD: Legacy audio disable: if 1, all legacy audio functions are disabled

JE: Enable joystick function at I/O address specified by Joystick base

I/O Registers

The base address mechanism provides 16 bytes of I/O to the device. These 16 bytes can be located in memory or I/O space.

Write Mode

Writing a byte from base + 0 to base + 15 will send it to the P16 FIFO for further processing by the P16. Actions taken are totally firmware-dependent.

Additionally, base + 2 is reserved for external EEPROM programming as follows:

7	6	5	4	3	2	1	0
						SDA	SCL

SDA and SCL are write-only. Writing to these bits will be immediately reflected in the corresponding SDA and SCL pins.

Read Mode

Two byte registers, data and status, are implemented respectively at base + 0 and base + 1.

When the P16 writes to the data register, an interrupt request is sent to the host processor. This request is cleared by the host reading the data register.

The status register format is as follows:

7	6	5	4	3	2	1	0
Dsr*	Drr	Sx2	Sx1	Sx0	0	0	0

Dsr*: 0 if data pending (asserts $\overline{INTA}$), set by read data (de-asserts $\overline{INTA}$)

Drr*: 0 if ready to accept data, 1 if P16 FIFO full

Sx2, Sx1, Sx0: bits which can be programmed by the P16, indicating the type of data pending.

EEPROM Format

Address	Data
00H	55H - First byte of EEPROM identification
01H	AAH - Second byte of EEPROM identification
02H	Vendor ID low byte (Config @ 00H)
03H	Vendor ID high byte (Config @ 01H)
04H	Device ID low byte (Config @ 02H)
05H	Device ID high byte (Config @ 03H
06H	Subsystem Vendor ID low byte (Config @ 2CH)
07H	Subsystem Vendor ID high byte (Config @ 2DH)
08H	Subsystem Device ID low byte (Config @ 2EH)
09H	Subsystem Device ID high byte (Config @ 2FH)
0AH	PMI Capability ID (Config @ 80H)
0BH	PMI Next Item Ptr (Config @ 81H), normally zero
0EH	PMI PMCSR low byte (Config @ 84H), only bits 2 to 7 used
0FH	PMI PMCSR high byte (Config @ 85H), only bits 5 and 6 used
10H	PMI PMCSR_BSE (Config @ 86H), normally zero
11H - 1FH	PMI Data

Timings

All timings conditions: V_{CC} = 5V, V_{C3} = 3.3V,T_A = 25°C

The SAM9777 complies with the PCI bus and AC-97 timings.

For PCI bus timings, please refer to *PCI Local Bus Specification. Rev 2.1, June 1, 1995*, published by the PCI Special Interest Group.

For AC-97 codec timing, please refer to *Audio Codec 97 Component Specification. Rev 1.03, Sept. 15, 1996*, published by Audio '97 Working Group;

Audio Codec 97, Rev 2.0, Sept. 29, 1997, published by Intel Corporation.

I2S Digital Audio

These timings refer to pins SD_OUT_0 to SD_OUT_2, SD_IN_0 to SD_IN_3, BCK_OUT, WS_OUT.

tck refers to the period of the CKIN clock (typically 81.38 ns).

Figure 3. Digital Audio Timing

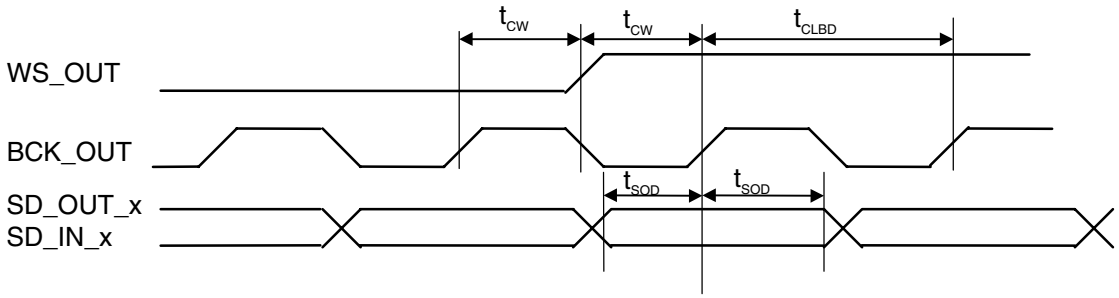
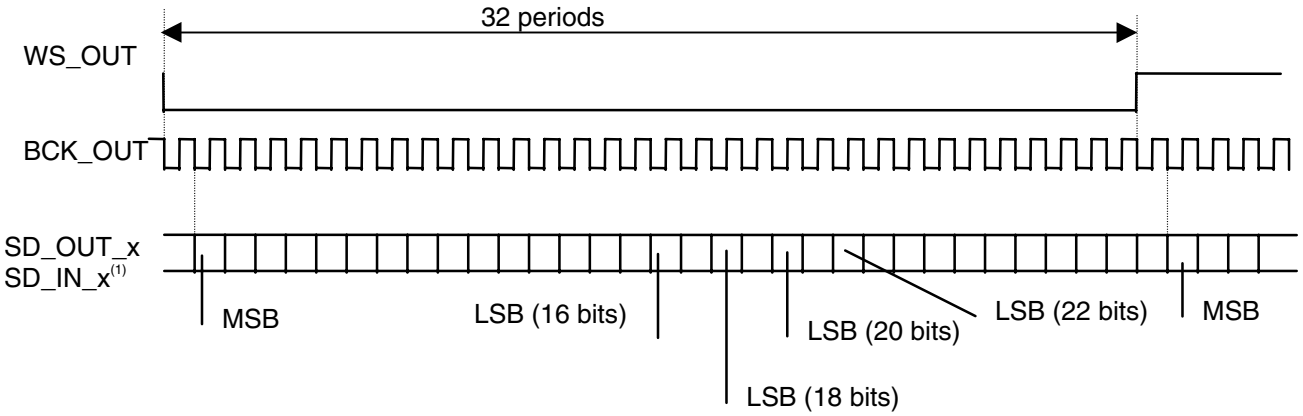


Table 14. Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{CW}	BCK_OUT rising to WS_OUT change	8•tck-10			ns
t_{SOD}	SD_OUT_x valid prior/after BCK_OUT rising	8•tck-10			ns
t_{CLBD}	BCK_OUT cycle time		16•tck		ns

Digital Audio Frame

Figure 4. Digital Audio Frame Format



Note: 1. SD_IN_x digital audio data is truncated to 20 bits.

EEPROM Timing

The SAM9777 complies with the Atmel AT24Cxx serial CMOS EEPROM.

A low-to-high transition of $\overline{RST}$ initiates the read EEPROM by sequentially reading addresses 0 to 31 from the EEPROM and storing corresponding data into internal registers.

The first two EEPROM bytes should be 55H AAH in order for the remaining 29 bytes of the loaded internal registers to be validated.

The serial clock SCL for the EEPROM is derived from the PCI bus clock CLK divided by 1024 (nominal 32.2 kHz).

The total read time for the EEPROM is 316 cycles (9.8 ms).

The EEPROM can be written to by directly controlling the SCL and SDA data lines at I/O byte base + 2. It is the responsibility of the programmer to generate the appropriate SCL and SDA timing.

Power-up/Reset/Power-down

The SAM9777 has a built-in PLL, allowing multiplication by 4 of an incoming clock frequency to provide the internal clock, the DSP clock and the P16 system clock.

When $\overline{RST}$ is low or if no clock signal is detected on the AC 97 CKIN, then the incoming clock frequency is CLK divided by 3 (11 MHz), which is raised by the PLL at 44 MHz.

When $\overline{RST}$ is high and a clock signal is detected on the AC'97 CKIN, then the incoming clock frequency is CKIN (12.288 MHz), which is raised by the PLL at 49.152 MHz.

Additionally, the P16 has the possibility of entering a soft power-down mode by dividing the system clock by 32. Depending on the firmware, the P16 can decide to enter this mode by itself in case there is no audio activity or do it under control of the host processor.

After a low-to-high transition of $\overline{RST}$, the P16 starts executing instructions from a built-in bootstrap ROM. This allows the upload of an initial firmware to the P16 local program/data RAM. This firmware will communicate with the host to establish the mapping with the host memory. Firmware execution can then start from host memory.

Recommended Board Layout, LFT Filter

The pinout of the SAM9777 has been organized for direct trace connection to the PCI connector with no need for a four-layer printed circuit board.

As per PCI specification, signal traces should be limited to 1.5 inches. The trace length for the PCI CLK signal should be 2.5 inches ± 0.1 inch.

- GND, V_{CC}, V_{C3} distribution, decouplings

All GND, V_{CC}, V_{C3} pins should be connected. GND + V_{C3} planes are strongly recommended below the SAM9707. The planes should be connected to all ground/+3.3V pins from the PCI connector.

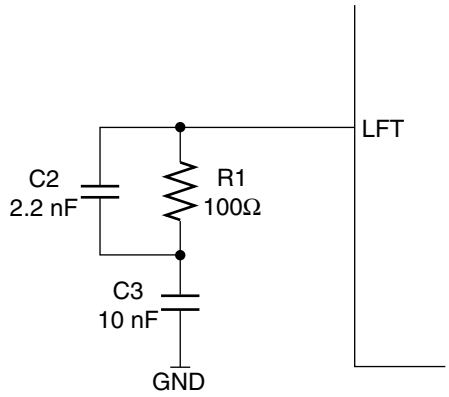
Recommended decoupling is 0.1 µF at each corner of the IC with an additional 10 µF bulk decoupling. V_{CC} requires a single 0.1 µF decoupling close to the IC.

- LFT

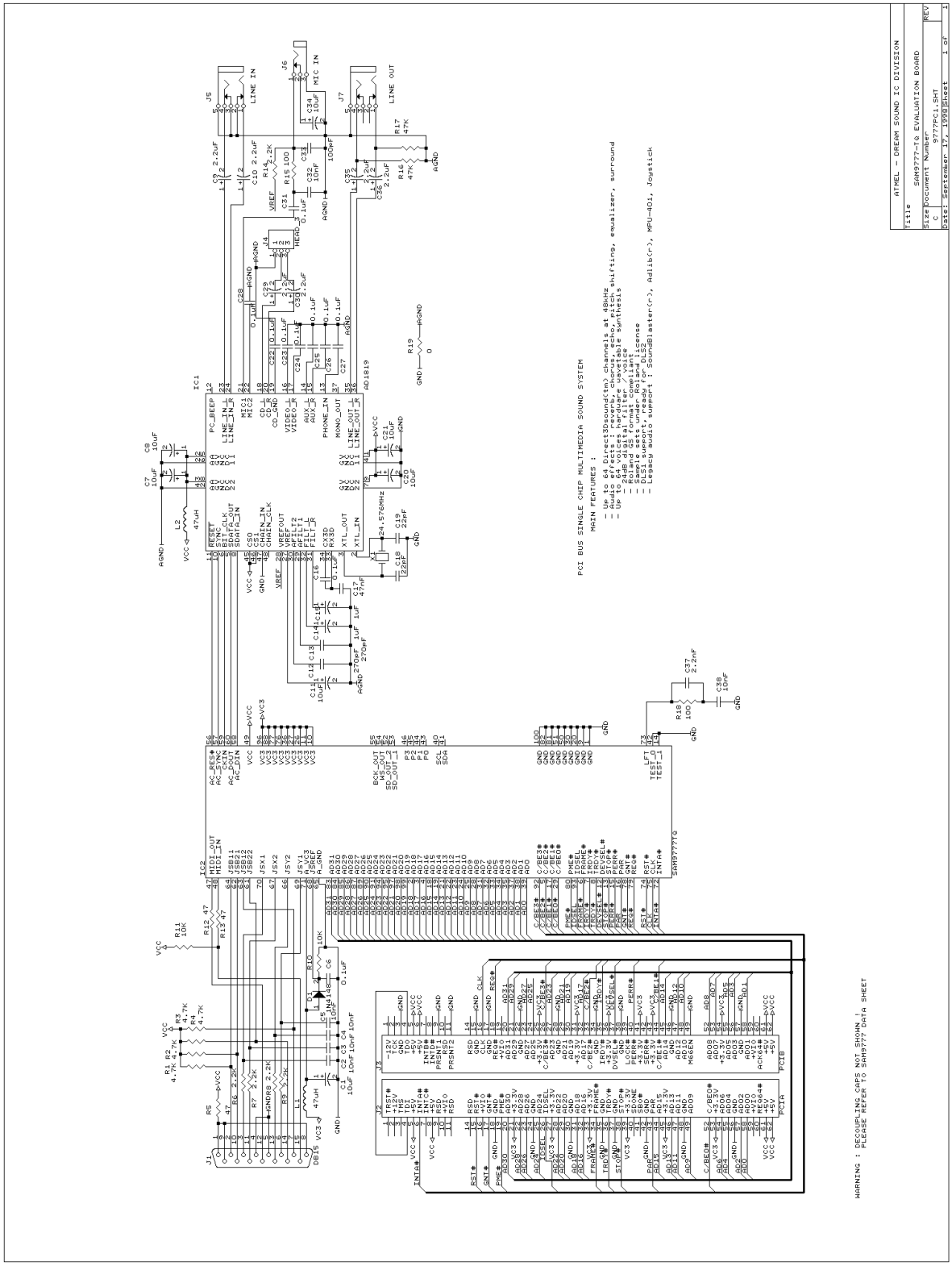
The paths between the LFT filter R-C-R and the SAM9777 should be short and shielded. The ground return from the LFT filter should be the GND plane from SAM9777.

The typical LFT filter is shown in Figure 5.

Figure 5. LFT Filter



Typical Design



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